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The USRP E310 offers a portable stand-alone SDR platform designed for field deployment. The flexible 2x2 MIMO AD9361 transceiver from Analog Devices provides up to 56 MHz of instantaneous bandwidth and spans frequencies from 70 MHz ? 6 GHz to cover multiple bands of interest.

- Xilinx Zynq 7020 SoC: 7 Series FPGA with ARM Cortex A9 667 MHz dual-core processor
- Analog Devices AD9361 RFIC direct-conversion transceiver
- Frequency range: 70 MHz - 6 GHz
- Up to 56 MHz of instantaneous bandwidth
- 2x2 MIMO transceiver
- Up to 10 MS/s sample data transfer rate to ARM processor
- RX, TX filter banks
- Integrated GPS receiver
- 9-axis inertial measurement unit

- SSB/LO Suppression -35/50 dBc
- Phase Noise 3.5 GHz 1.0 deg RMS
- Phase Noise 6 GHz 1.5 deg RMS
- Power Output >10dBm
- IIP3 (@ typ NF) -20dBm
- Typical Noise Figure <8dB

- 133 x 68 x 26.4 mm

- E310 0-40 °C

E310 Schematics

E310 DB

TXS02612RTWR

XC7Z020-1CLG484CES9919

USB3340-EZK-TR

AK4571VQP

FT230XQ-R

88E1512

24LC024/SN

DS1339,SM

ADT7408

MPU-9150

BMP180

BQ24192

TPS54478

MAX6510HAUT-T

[ATTINY88-MU](#)

[TPS61253YFF](#)

[AD9361 Product Page](#)

[Xilinx Zynq Product Page](#)

[InvenSense MPU-9150 Product Page](#)

Request a detailed whitepaper covering features and components from info@ettus.com

- Partial Enclosure 225 g
- Full Enclosure 375 g

- E310 Drawings - [File:E310 Dimensional Sketches.pdf](#)

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- 10/100/1000 BASE-T Ethernet
- Stereo audio out, mono mic in
- Integrated GPS receiver
- Host USB support
- 9-axis IMU

[ADD E310 FPGA IMAGES]

[FPGA Resources](#)

[UHD Stable Binaries](#)

[UHD Source Code on Github](#)

- [USRP E310 Architecture](#)