QR210 Architecture and Overview

Contents

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The QR210 is a four-channel receiver designed for signals intelligence (SIGINT) and spectrum monitoring applications. It is intended to be used as phase array receiver, where all of the channels are tuned to the same frequency. Phased-array processing can enables several modes of operation including: beamforming, interference cancellation, and direction finding. This document will provide an overview of the QR210 architecture.

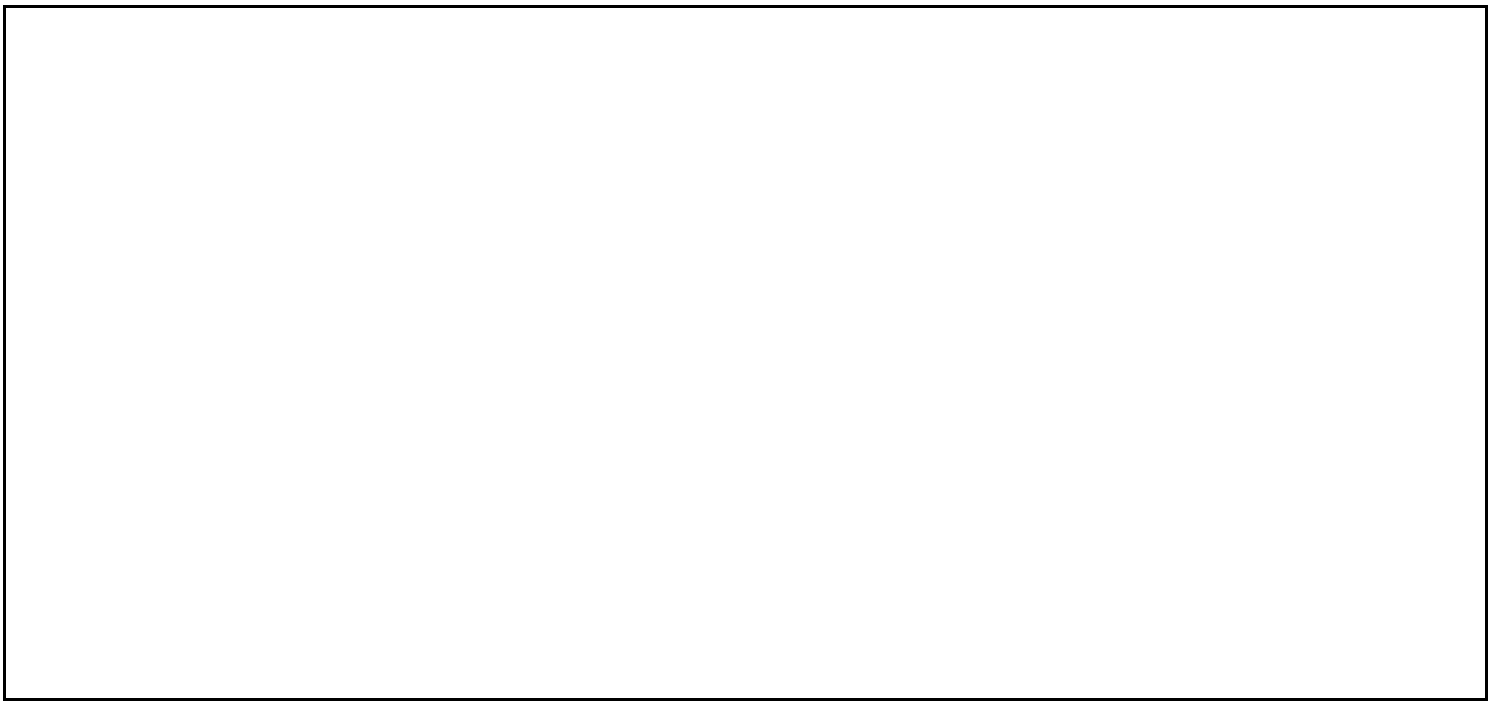

Figure 1 - QR210 Quadradio - 4-Channel Receiver

The architecture of the QR210 can be seen in Figure 2. The three key subsystems are:

1. RF Frontend Modules ? Provide filtering, amplification, down-conversion, and digital sampling of the RF signals.
2. LO/Cal Distribution Subsystem ? Generates the local oscillator and calibration signals that are distributed to each RF front end. Includes provisions for external LO/Cal distribution for multi-unit systems.
3. FPGA/Power/Clocking Subsystem ? Provides high-performance FPGA, host interfaces, power regulation, 10 MHz clock generation, and sample clock generation.

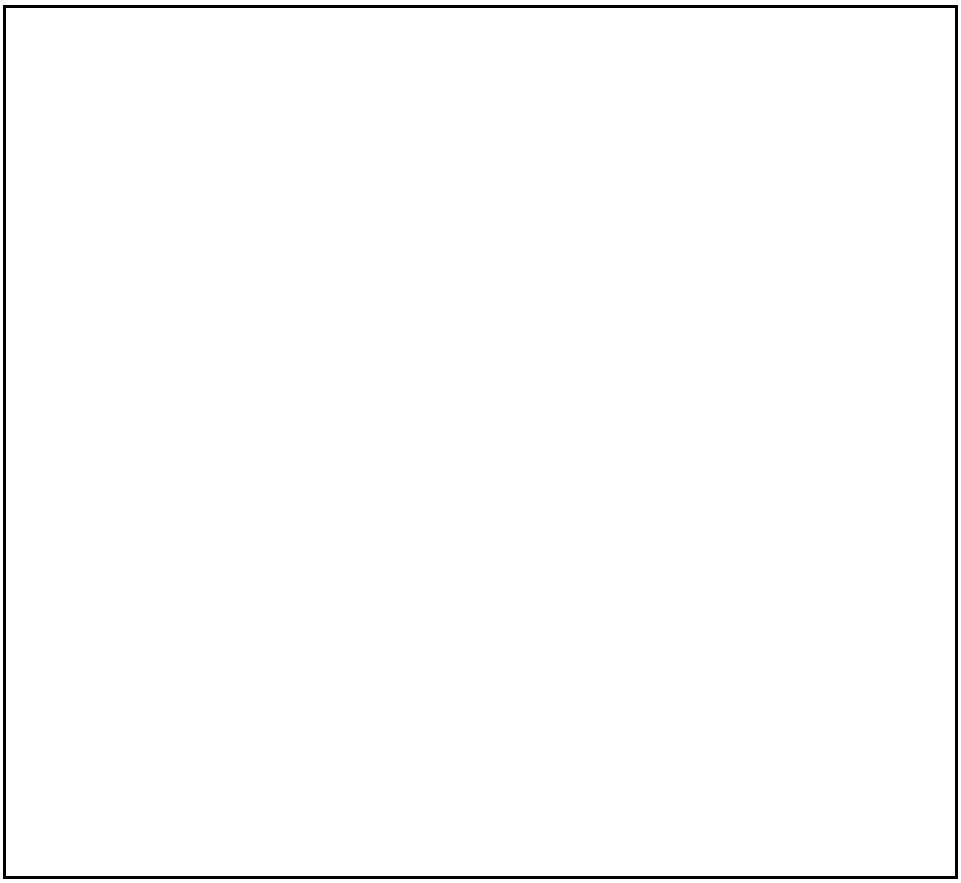

Figure 2 - High Level Block Diagram

The QR210 contains four frontend receive modules per unit. Each receive module functions independently, but all modules are driven by a common local oscillator, calibration source, and sample clock to ensure coherency. The module was split into two block diagrams, Figure 3 and Figure 4, for clarity.

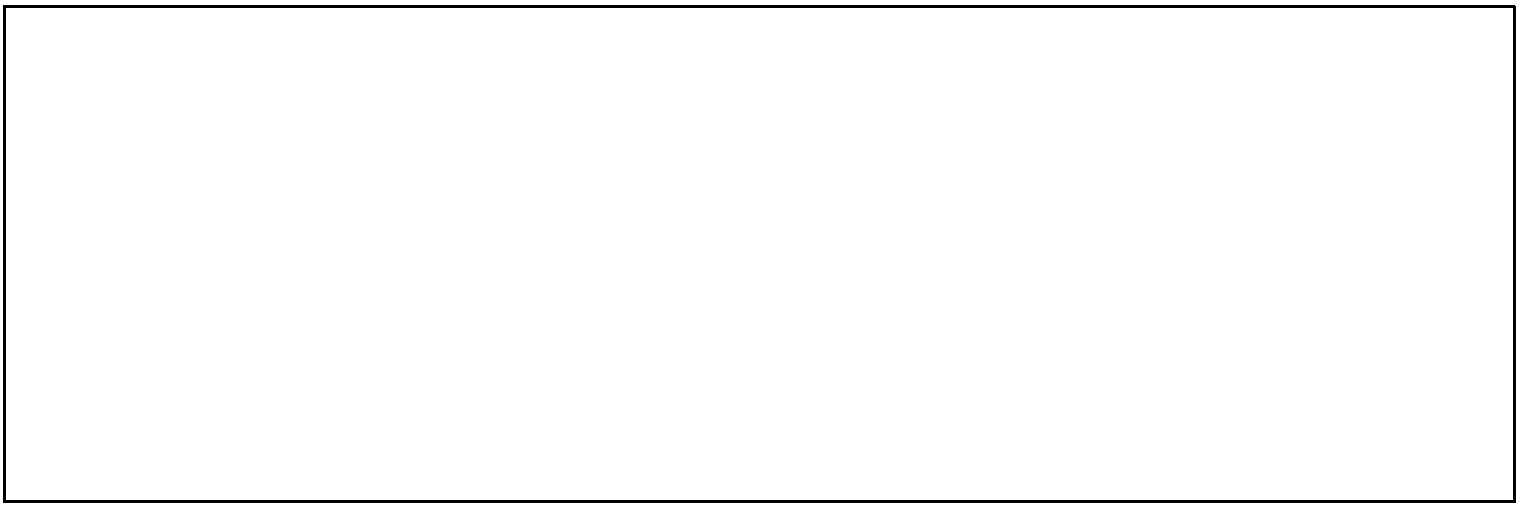

Figure 3 - Receive Front End Module - Filter Bank

The first component in the signal chain is an RF switch, which selects the RF input signal or the internal calibration signal. This allows the system to perform loop-back test and calibration without disconnecting any external components. The calibration signal is used to correct quadrature imbalances, local oscillator leakage, and channel-to-channel phase/amplitude offsets.

After selecting the signal source, the front end passes the signal through a switched filter bank. The filter bank rejects strong out of band interference. In order to minimize the Noise Figure(NF) of this front end, the signal undergoes amplification after the first bandpass filter. A programmable attenuator allows adjustment of the receiver's cascaded gain. The signal passes through a second amplifier prior to a matched bandpass filter.

In stock configuration, the 6 bands that can be selected are:

Band	Frequency Min (GHz)	Frequency Max (GHz)
A	0.700	1.00
B	1.00	1.50
C	1.50	2.20

D	2.20	3.00
E	3.00	3.50
F	3.50	4.00

Table 1 - RF Band Frequency Limits

The remainder of the signal path is common for all bands. After the filter bank, a second adjustable attenuator provides an additional gain adjustment range. The signal is then down-converted to complex-baseband. This mixer is driven by the system LO, which is shared across all front ends. The resulting complex baseband signal passes through a 50 MHz filter. The filtered baseband signal is sampled by a 16-bit, 120 MS/s ADC.

There are several ancillary components that aid in the operation of the front end. An on-board CPLD serves as a port expander, providing all of the outputs necessary to control switches, attenuators, etc. There is also a temperature sensor that can be used for temperature compensation of the frontend in the digital domain.

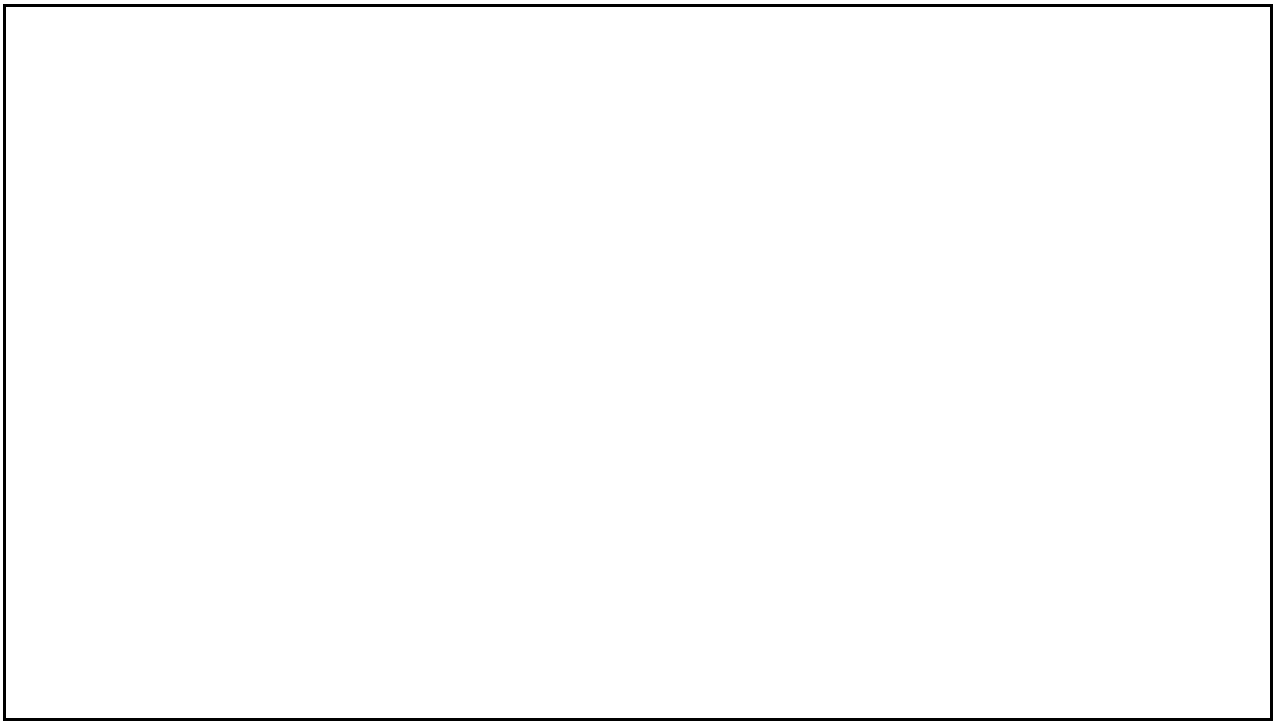

Figure 4 - Receiver Front End Module ? Down-Conversion and ADC

The LO and Cal Distribution Subsystem (Caldiv) accepts reference clocks from the main board, synthesizes the shared LO and Cal signals, and distributes these signals to the RF frontends with matched-length paths.

The Caldiv board accepts a 10 MHz reference input that is used in both the Calibration signal and LO synthesizers. A YIG-tuned oscillator accepts the 10 MHz reference input and generates an output in the frequency range of 3 to 9 Ghz. In order to cover the frequency range from 700 MHz to 4 GHz, a divider is used to reduce the frequency output of the YIG-oscillator. After division, the signal is amplified. A four-way filter bank is used to provide rejection of harmonics across the full frequency range. The signal is then passed through a switching network that allows the LO signal to be output for external distribution. The circuit can also accept an external LO as an input. This enables larger systems of QR210s to be built with external distribution of the LO. After selecting internal/external LOs, the signal is split into four directions with a passive splitter. Matched length traces bring the signals to four SMA connectors.

The calibration (Cal) signal in this system is an un-modulated tone that is distributed to all of the front ends. The generation and distribution of the calibration signal is similar to that of the LO. The only difference is the divider is integral to the PLL IC that is used to generate the Cal signal. Thus, no additional dividers are required.

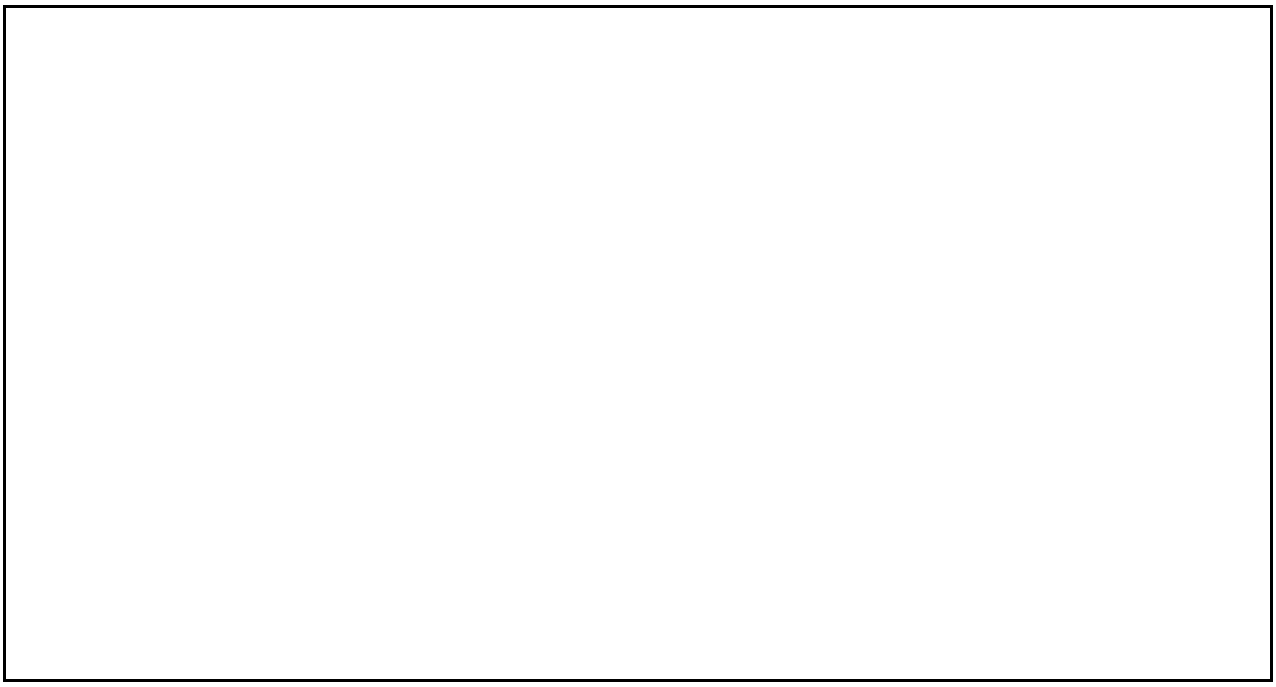

Figure 5 - Caldiv Block Diagram

The main board provides power regulation (not shown), host-interfaces, clock generation, and the digital processing capability used to operate the QR210. A block diagram of the Main Board can be seen in Figure 6. The core of the Main Board is the V5SXT95T FPGA, which handles low-level control, all host-interfaces, and DSP operations such as filtering, decimation, and beamforming.

Two SFP+ connectors provide a 1 Gigabit and 10 Gigabit Ethernet interfaces. These SFP+ connectors use external adaptors to allow connection of standard copper or optical cables. A DB-9 connector provides an RS-232 interface for general, low-speed debugging capability. There is hardware for PCIe and MIMO interfaces, but these are not implemented in the FPGA or host driver.

An auxiliary DAC is used as a signal generator. In the stock configuration, this will be used to generate an IF that contains a re-modulated result of the DSP0 Beamformer output.

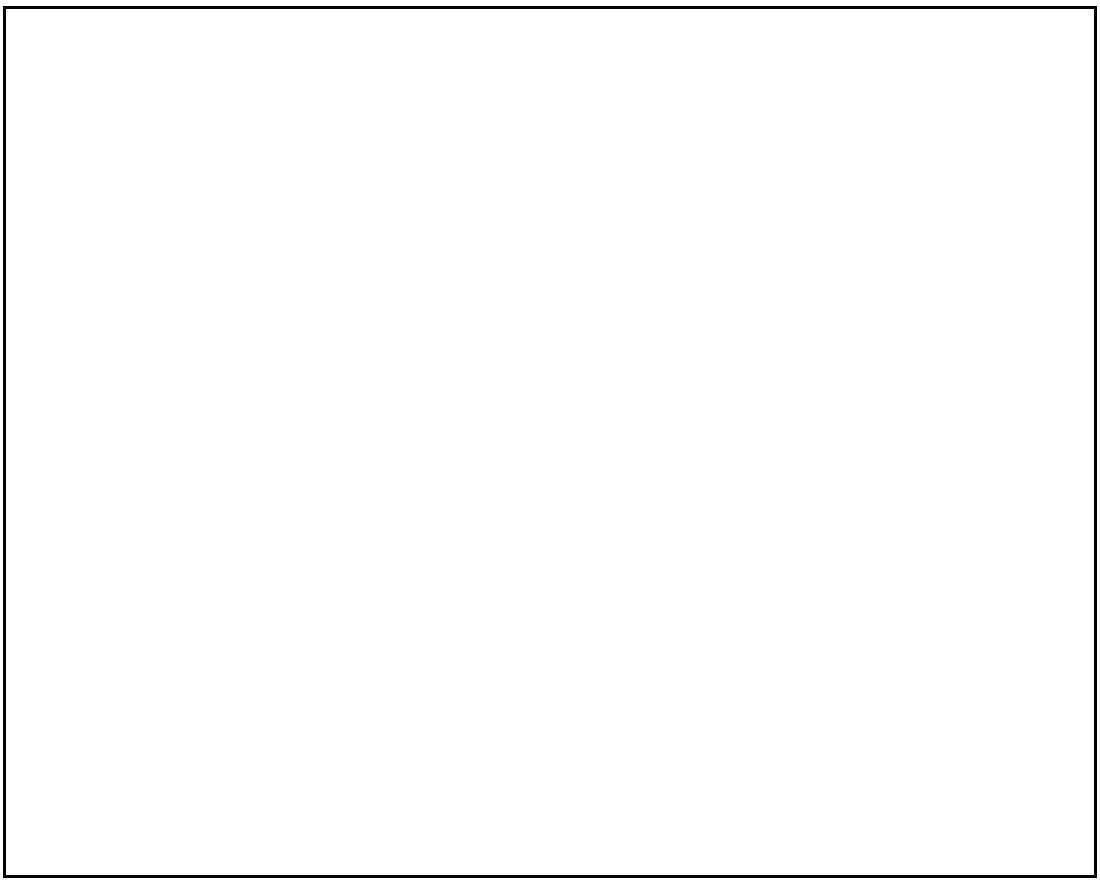

Figure 6 - Main Board Block Diagram

The clock generation circuitry has been designed to allow the greatest level of flexibility for coherent systems. The system's 10 MHz reference is selected from several sources: internal GPSDO, external input, or MIMO cable (not implemented). When more than one QR210s are integrated into a system, the 10 MHz Ref. Output can be distributed using an external splitter and matched length cables to all units. The 10 MHz output will be "looped

back" through this distribution network to the QR210 that provides the reference. Latter sections will provide a better illustration of this configuration.

The 10 MHz reference is output to the LO/Cal generation (Caldiv) board through an SMA connector. It also serves as a reference for the ADC sample clock generator. This is an Integer-N PLL that multiplies the 10 MHz reference to 120 MHz. The 120 MHz signal is distributed to the digital front end interface via matched-length traces to ensure sample clock alignment on all channels.

While the user has the freedom to modify the FPGA to meet their particular application requirements, Ettus Research has developed and will provide a default personality for the QR210. This default personality provides the following functions:

1. Implementation of internal interfaces for command and control of the radio
2. Implementation of Host Interface ? including 1 GigE and 10 GigE
3. DSP operations ? frequency selective I/Q compensation, DC correction, decimation, etc.
4. VITA-49 Framing and Time-Stamping of all data

A block diagram of the stock DSP functionality is shown in Figure 7. I/Q samples are received from each front end at 120 MS/s. The first step in the DSO chain is a decimate-by-2, which reduces the sample rate to 60 MS/s. Next, DC offset correction is applied with an IIR. This function can be disabled, or locked to a constant value after calibration. Next, a frequency selective I/Q correction is applied to reduce I/Q imbalance across the bandwidth of the baseband signal. The coefficients of this filter can be changed based on calibration routines developed by Ettus Research.

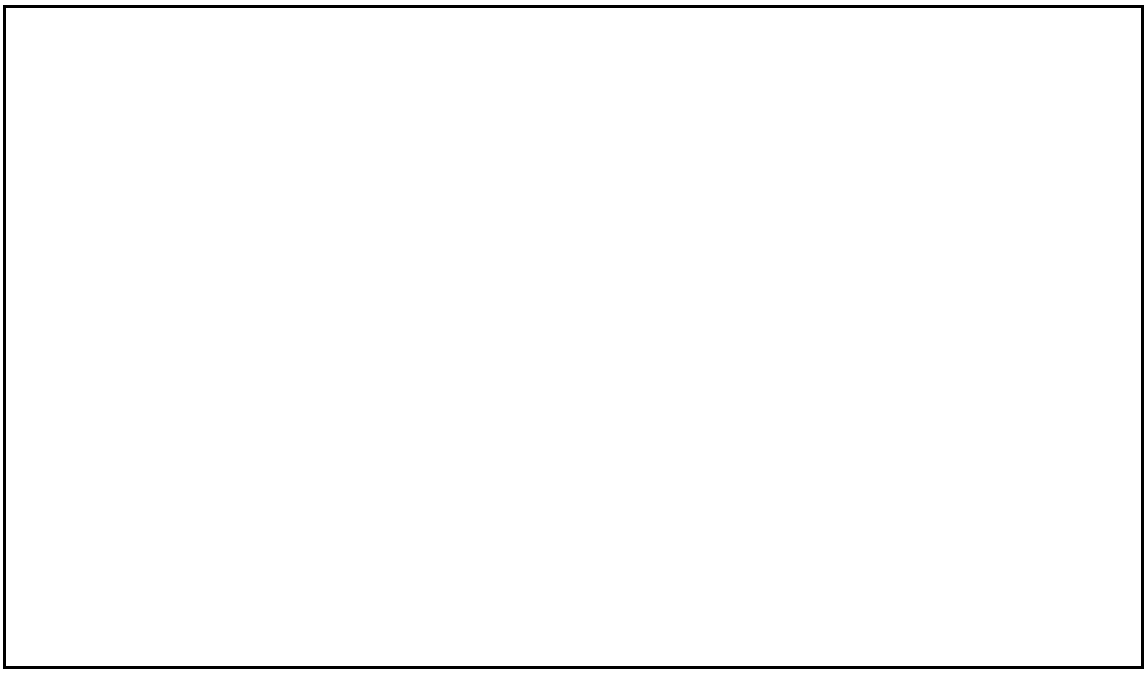

Figure 7 - Stock DSP Configuration

The output of each channel's I/Q correction block are fed to four beamformers. These beamformers are implemented by performing a complex multiplication of each channel with user-configurable complex taps. If the user wishes to use the raw samples from each DSP chain, the coefficients for this multiplies would be set to {1,0,0,0} for Channel 0, {0,1,0,0} for Channel 1, etc. Additional decimation is performed by configurable half-band filter banks, the provide decimation factors of 1, 2, 4, or 8. These four beamformed streams are each passed to independent VITA-49 framers. All four Framers output to the1 GigE and 10 GigE Packet Router.

The QR210 is supported by the UHD? (USRP Hardware Driver) programming interface. This allows the user to configure and stream samples from the receiver in a similar way to the other USRP products. The driver provides a C++ API for these functions. This API is also used by GNU Radio blocks, which allow developers to build software receivers in GNU Radio Companion.

While each QR210 contains four receive channels, up to eight QR210s can be "stacked" to provide a 32-input system. For more information about these multi-QR210 systems, please see Building a 32-Channel System with the QR210.

The QR210 was designed with high-performance RF frontends that include pre-select filter banks, a wideband quadrature downconverter, and a 16-bit, 120 MS/s. This allows the developer receive up to 50 MHz of bandwidth with high dynamic range. The shared YIG-tuned LO signal and internal calibration signals allow rapid calibration of the QR210 and assure coherenecy and channel-to-channel alignment. The Virtex-5 FPGA provides ample resources for sophisticated signal processing applications, and the UHD software API allows users to rapidly develop in graphical, software-defined environments. For more information, please visit the QR210 product page, or the additional resources provided below.

Link: Building a 32-Channel System with the QR210

Link: QR210 Product Page