X310

Contents

- 1 Device Overview
- 2 Key Features
  - 2.1 X300
  - 2.2 X310
- 3 Compatible Daughterboards
- 4 RF Specifications
  - 4.1 RF Performance (with SBX-120)
- 5 Physical Specifications
  - 5.1 Dimensions
- 6 Environmental Specifications
  - 6.1 Operating Temperature Range
- 7 Schematics
  - 7.1 X300/X310
- 8 Datasheets
- 9 Mechanical Info
  - 9.1 Weight
  - 9.2 Drawings
- 10 FPGA
- 11 Interfaces and Connectivity
- 12 Downloads
- 13 Application Notes
- 14 FAQ

The Ettus Research USRP X310 is a high-performance, scalable software defined radio (SDR) platform for designing and deploying next generation wireless communications systems. The hardware architecture combines two extended-bandwidth daughterboard slots covering DC ? 6 GHz with up to 120 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA in a convenient desktop or rack-mountable half-wide 1U form factor.

- Xilinx Kintex-7 XC7K325T FPGA
- 14 bit 200 MS/s ADC
- 16 bit 800 MS/s DAC
- Frequency range: DC - 6 GHz with suitable daughterboard
- Up 120MHz bandwidth per channel
- Two wide-bandwidth RF daughterboard slots
- Optional GPSDO
- Multiple high-speed interfaces (Dual 10G, PCIe Express, ExpressCard, Dual 1G)

- Xilinx Kintex-7 XC7K410T FPGA
- 14 bit 200 MS/s ADC
- 16 bit 800 MS/s DAC
- Frequency range: DC - 6 GHz with suitable daughterboard
- Up 120MHz bandwidth per channel
- Two wide-bandwidth RF daughterboard slots
- Optional GPSDO
- Multiple high-speed interfaces (Dual 10G, PCIe Express, ExpressCard, Dual 1G)

- WBX-120 / WBX-40
- SBX-120 / SBX-40
- CBX-120 / CBX-40
- UBX-160 / UBX-40
- BasicTX / BasicRX
- LFRX / LFTX

- SSB/LO Suppression -35/50 dBc
- Phase Noise 3.5 GHz 1.0 deg RMS
- Phase Noise 6 GHz 1.5 deg RMS
- Power Output >10dBm
- IIP3 (@ typ NF) 0dBm
- Typical Noise Figure 8dB

27.7 x 21.8 x 3.9 cm

- X300/X310 0-40 °C

X300/X310 Schematics

- XC7K325T
- XC7K410T
- FPGA - XC7K410T-2FFG900
- FPGA - XC7K410T-2FFG900

- 12-Bit ADC - AD7922ARMZ

- 12-Bit DAC - AD5623RBRMZ-3
- Dual Channel, 16-Bit, 1230 MSPS DAC - AD9146
- Dual Channel, 14-Bit 210 MSPS ADC - ADS62P48
- High Speed Differential Receiver - FIN1002
- EEPROM - 24LC256T
- Jitter Cleaner With Dual Loop PLLs - LMK04816BISQ/NOPB_1/3
- MULTIPLEXER - SY89547LMGTR
- Single Schmitt-Trigger Buffer Gate - SN74AUP1T17
- SHIELD-748871-01
- NUP4302
- Synchronous Step Down SWIFT? Converter - TPS54620RGYT
- Regulator - LT1764EQ-3.3
- Voltage Regulator - TPS7A47
- Monolithic Synchronous Step-Down Regulator - LTC3603EUF_TRPBF
- LOW-DROPOUT VOLTAGE REGULATORS - TPS77625_SM
- TPS511116
- LOW-DROPOUT LINEAR REGULATORS - TPS79318_SM
- HDR2X7-761985-01
- FT223HQ

With 2x SBX-120: 1.7kg

Resource Type	X300 - XC7K325T			X310 - XC7K410T		
	Count	Total	Available	Count	Total	Available
DSP48 Blocks	753	840	90%	1453	1540	94%
Block Rams (18 kB)	5	445	1%	356	795	45%
Logic Cells	125536	203800	62%	182024	254200	72%
Slices LUTS	27413	50950	54%	38801	63550	61%

- Updated February 18, 2014 for UHD 3.8.5

Follow the links below for additional information on configuring each interface for the USRP X300 or X310 SDRs.

- Dual 10 Gigabit Ethernet - 200 MS/s Full Duplex @ 16-bit
- PCIe Express (Desktop) - 200 MS/s Full Duplex @ 16-bit
- ExpressCard (Laptop) - 50 MS/s Full Duplex @ 16-bit
- Dual 1 Gigabit Ethernet - 25 MS/s Full Duplex @ 16-bit

FPGA Resources

UHD Stable Binaries

UHD Source Code on Github

- USRP X300 and X310 Configuration Guide
- Guide for the USRP X300/X310 GPIO Expansion Kit
- Guidance on SFP+ Adapters for Fiber Connectivity on USRP X300/X310
- USRP X Series Quick Start (Daughterboard Installation)

https://www.ettus.com/kb/detail/usrp-x300x310-faq

USRP? X300 and USRP? X310 SDRs Frequently Asked Questions

- **What is the bandwidth of the USRP X300/X310**

The ADC rate on each analog RX channel is 200 MS/s quadrature, which provides a theoretical analog bandwidth of approximately 80% of the Nyquist bandwidth of +/- 100 MHz (+/- 80 MHz around the center frequency). The resulting maximum theoretical analog bandwidth is 160 MHz. The actual analog bandwidth may be reduced due the RF daughterboard selected.

RF Daughterboard Bandwidths: See the daughterboard specifications [link]

FPGA Processing Bandwidth: Up to 200 MS/s quadrature.

Host Bandwidth: Up to 200 MS/s quadrature, dependent on selected interface

For more information about achieving the maximum bandwidth with a USRP X300/X310, please see the "USRP X300/X310 Configuration Guide" or the "USRP System Bandwidth" application note.

- **How can I program the USRP X300/X310**

Like all other USRP models, the USRP X300 and X310 are compatible with the USRP Hardware Driver? (UHD) architecture. The UHD architecture is a common driver that allows users to develop and execute applications on a host-PC. UHD provides a direct C++ API to control and stream to/from the USRP X300/X310. It also provides compatibility with a variety of third-party software frameworks including GNU Radio, Labview, and Matlab. You may also customize the FPGA image provided with UHD to integrate your own signal processing. For more information about UHD, and supported software frameworks, please see:

http://files.ettus.com/manual/

- **How do I update the FPGA images and firmware with the latest from UHD**

You can find more information about updating the FPGA image through PCIe, 1/10 GigE, and JTAG here.

- **How can I modify the FPGA of the USRP X300/X310**

The source code (Verilog) for the USRP X300/X310 is available in the UHD repository. The USRP X300/X310 requires ISE 14.4 or newer. The build process leverages the existing CMAKE build system used to compile the host-side driver. A Linux-based setup will provide the best results.

- **How much free space is available in the USRP X300/X310 FPGA**

Please see the USRP X300/X310 FPGA resources page for more information.

- **What type of PC setup is recommended for use with the USRP X300/X310**

The type of PC required depends heavily on the complexity and bandwidth of the application. To demonstrate the USRP X300/X310, we typically use a desktop computer with a quadcore i7, 8+ GB of DDR3, and install the PCIe interface card that is also provide with the 10 GigE, PCIe, and ExpressCard interface kits.

- **What frequency range does the USRP X300/X310 cover**

The frequency range depends on the daughterboard select by the users. For more information, please see the USRP X300/X310 Configuration Guide.

- **What components do I need to purchase for a complete USRP X300/X310 system**

For a more comprehensive guide, please see the USRP X300/X310 Configuration Guide.

- **What is the difference between the USRP X300/X310**

The USRP X310 includes a larger Kintex-7 series FPGA (XC7K410T) with additional development resources for more complex designs. The USRP X300 includes the smaller XC7K325T FPGA.